

SYNCHRONOUS MIRROR DELAY CIRCUIT AND SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE HAVING THE SAME

ABSTRACT OF THE DISCLOSURE

5

Disclosed is a synchronous mirror delay circuit for generating an internal clock signal synchronized with an external clock signal, comprising: a clock buffer circuit that generates a reference clock signal in response to the external clock signal; a delay monitor circuit that delays the reference clock signal; a forward delay array for delaying an output clock signal of the delay
10 monitor circuit to generate delay clock signals; a mirror control circuit that receives the delay clock signals and the reference clock signal to detect one delay clock signal synchronized with the reference clock signal among the delay clock signals; a backward delay array that delays the delay clock signal detected by the mirror control circuit to output a synchronous clock signal; a
delay circuit that delays an asynchronous clock signal output through the forward delay array;
15 and a clock driving circuit that outputs the delayed asynchronous clock signal as the internal clock signal when the reference clock signal is not synchronized with one of the delay clock signals.